REMARKS

Reconsideration of the application is requested.

Claims 1-9 remain in the application. Claims 1-9 are subject to examination.

In the second paragraph on page 2 of the above-identified Office Action, the Examiner objected to drawings for not showing the common interface between the semiconductor region 2 and the second insulating layer 4. The Examiner is believed to be reading the claim incorrectly. The semiconductor region, in claim 1, is recited to be the well 2. The well 2 shares a common border or interface with the second insulating region 4.

The varactor of the instant application is based on a metal oxide semiconductor (MOS) structure normally having an active area with adjacent source and drain areas as well as on top, a gate electrode separated from the active area by an insulating layer. Instead of a source and drain area placed to the right and to the left of n-well 2, the present varactor contains a well terminal region 6 for connecting to the semiconductor region. The well terminal region 6 may be embodied in the form of a so-called collector deep implantation area which is n+ doped, meaning that it is

higher doped than the n-well 2. Furthermore, to better insulate the active n-well region 2, a first insulating area 3 is provided next to the n-well 2. The first insulating area 3 is also disposed next to the second insulating region 4 which may for example be embodied as a shallow trench insulation (STI). Consequently, we believe that there can be no doubt about the fact that the n-well 2 and the second insulating region 4 share a common, bordering surface, namely on the surface of the semiconductor body 2. The bordering surface between the n-well 2, namely the semiconductor region 2, and the second insulating region 4 is not only shown in Fig. 2, but can also be seen in Fig. 1 and in Fig 4 of the drawing.

We further note that the resistors and capacitors shown in Fig. 1 are diagrammatic elements for helping to understand the function of the integrated varactor structure according to the invention as shown in Fig. 2.

For the above-stated reason, the Examiner is respectfully requested to withdraw the drawing objection.

In the first-fourth paragraphs on page 3 of the above-identified Office Action, claims 1-9 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

The Examiner states that the claim presents multiple elements in the claimed invention but fails to indicate which elements make up the claimed invention. In addition, the Examiner requests that the first and second capacitive plates and the associated dielectric layer be identified.

First it is stated that all of the features recited in the claims make up the tunable capacitance. Second, it is respectfully pointed out that the invention of the instant application does not refer to a conventional plate capacitor, but rather to an integrated capacitive structure formed in a semiconductor fabrication process.

Capacitors in integrated form are widely used and are described in many papers some of which are cited in the "Field of the Invention" section of the instant application. For example, the paper by Wallace Ming Yip Wong et al., entitled "A Wide Tuning Range Gated Varactor", shows in Figs. 1 band 1c a MOS varactor. There, it is clearly stated that the gate electrode of the varactor is one of the two electrodes, while the source and drain regions that are interconnected together, form the second electrode.

In the instant application, claim 1 recites that the capacitance is formed by the gate electrode which functions

as one of the electrodes, while the other electrode is formed by the well terminal region which has a higher dopant concentration. In the embodiment according to Fig. 2, the two electrodes would be formed by the gate 5 and the collector deep implantation area 6, as an example.

The fact, that the areas mentioned above form the two electrodes of the capacitor, are also explicitly disclosed on page 15, lines 8 to 17 of the specification of the instant application.

It is accordingly believed that the claims meet the requirements of 35 U.S.C. § 112, second paragraph. The above-noted changes to the claims are provided solely for clarification or cosmetic reasons. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In view of the foregoing, reconsideration and allowance of claims 1-9 are solicited.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith

should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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REL:cgm

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